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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/601,222	06/20/2003	Joseph M. Jeddeloh	501176.01	9072

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EXAMINER	
BROWN, MICHAEL J	

ART UNIT	PAPER NUMBER
2116	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/601,222	JEDDELOH ET AL.	
	Examiner	Art Unit	
	Michael J. Brown	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 July 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *48-124* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *48-124* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 April 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/30/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 7/30/2007 has been entered.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 7/30/2007 was filed. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Objections

3. Claim 48 is objected to because of the following informalities: Claim 48, line 7 reads "memory modules generating memory the output signals....". Examiner believes this should read "memory modules generating the memory output signals.....". Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 48-124 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leddige et al.(US Patent 6,477,614) in view of Volk(US Patent 5,388,265) further in view of Fung(US PGPub 2005/0177755).

In reference to claims 48, 74, and 100.....

Leddige discloses a system, computer system(computer system 100, see Fig. 1) and method for controlling power, comprising a processor(processor 101, see Fig. 1), an input device(keyboard interface 132, see Fig. 1), operably connected to the processor, allowing data to be entered into the computer system, an output

device(audio controller 133, see Fig. 1), operably connected to the processor, allowing data to be output from the computer system, and a memory system(memory 113, see Fig. 1), operably coupled with the processor. Leddige also discloses the memory system comprising a memory controller(memory controller 111, see Fig. 5), a memory bus(first memory bus 500, see Fig. 5) operably coupled with the memory controller to communicate memory commands from the memory controller and communicate memory output signals to the memory controller, and a plurality of memory modules(memory modules 210c, 211c, and 212c, see Fig. 5) operably coupled with the memory bus, the memory modules generating memory the output signals and responsive to the memory commands. Leddige further discloses at least some of the memory modules comprising an insulative substrate supporting a system interface(motherboard 200, see Fig. 2), a plurality of memory devices(memory devices 501, see Fig. 5) disposed on the insulative substrate, and a memory hub(memory repeater hub 520, see Fig. 5) disposed on the insulative substrate and operably coupled with the memory devices and the system interface, the memory hub managing communications between the memory devices and the system interface in response to memory commands received via the system interface.

However, Leddige fails to disclose the system, computer system, or method comprising an activity sensing device monitoring activity of the memory module containing the activity sensing device in processing memory commands, the activity sensing device being operable to generate an output corresponding thereto, and a module power controller coupled to the activity sensing device of the memory module

containing the module power controller, the module power controller being operable to direct the memory module containing the module power controller to a reduced power state responsive to the output of the activity sensing device indicating activity of the memory module containing the module power controller is not of a desired level.

Volk teaches an activity sensing device(power management logic 205, see Fig. 2) monitoring activity of a memory module(chip 200, see Fig. 2) in processing memory commands and generating an output corresponding thereto(see column 4, lines 52-54), and a module power controller(power management logic 205, see Fig. 2) operable to direct the memory module to a reduced power state(power down state; see column 4, line 55) responsive to the output of the activity sensing device indicating activity of the memory module is not of a desired level(see column 4, lines 54-55). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the inventions of Leddige and Volk in order to create a computer system with memory module monitoring means. The motivation to do so would be to establish an ability to conserve power when there is inactivity within a particular memory module.

In reference to claims 49, 75, and 101....

Volk teaches the system, computer system, and method wherein the module power controller directs the memory module to the reduced power state when the activity sensing device indicates memory module activity has fallen below the desired level(see column 5, lines 7-15).

In reference to claims 50, 76, and 102....

Volk teaches the system, computer system, and method wherein the module power controller directs the memory module to the reduced power state when the activity sensing device indicates memory module activity has exceeded the desired level(see column 5, lines 7-15).

In reference to claims 51, and 77, and 103....

Volk teaches the system, computer system, and method wherein the module power controller is operable to determine when the memory module should be directed to the reduced power state responsive to the output of the activity sensing device(see column 5, lines 7-15).

In reference to claims 52, 78, and 104....

Volk teaches the system, computer system, and method wherein the module power controller is operable to direct the memory module to the reduced power state upon receiving an external reduced power signal(see column 5, lines 7-15).

In reference to claims 53, 54, 79, and 80....

Volk teaches the system, computer system and method wherein the module power controller comprises a master power controller, the master power controller receiving the output of the activity sensing device from at least one other memory module and, responsive to the output of the activity sensing device indicating activity of

the memory module is not of the desired level, generates an external reduced power signal to direct the at least one other memory module to the reduced power state(see column 5, lines 7-15).

In reference to claims 55, 81, and 109....

Volk teaches the system, computer system, and method wherein the memory module is directed to the reduced power state by the module power controller responsive to a single indication the activity of the memory module is not of the desired level reflected in the output of the activity sensing device(see column 5, lines 7-15).

In reference to claims 56, 82, and 110....

Volk teaches the system, computer system, and method wherein the memory module is directed to the reduced power state by the module power controller responsive to a plurality of indications the activity of the memory module is not of the desired level reflected in the output of the activity sensing device(see column 5, lines 7-15).

In reference to claims 57, 83, and 111....

Volk teaches the system, computer system, and method wherein the memory module is directed to the reduced power state by the module power controller when the output of the activity sensing device indicates the memory module has not received memory commands for a predetermined time period(see column 5, lines 7-15).

In reference to claims 58, and 84....

Volk teaches the system, computer system, and method wherein the activity sensing device comprises an activity monitor that monitors memory commands directed to the memory module(see column 5, lines 7-15).

In reference to claims 59, and 85....

Volk teaches the system, computer system, and method wherein the activity monitor monitors the memory commands received via the system interface(see column 5, lines 7-15).

In reference to claims 60, 86, and 112....

Volk teaches the system, computer system, and method wherein the activity monitor comprises part of the memory hub(bus 202 see Fig. 2).

In reference to claims 61, 87, and 113....

Leddige in view of Volk discloses the system, computer system, and method as cited and explained above. However, Leddige and Volk fail to disclose the system, computer system, and method wherein the activity sensing device comprises a temperature sensor wherein the temperature sensor is operable to measure when the activity of the memory module is not of the desired level by monitoring temperature.

Fung teaches an activity sensing device(system, see paragraph 0149, sentence 111) comprising a temperature sensor(temperature sensor, see paragraph 0149, sentence 111) wherein the temperature sensor is operable to measure when the activity of the memory module is not of the desired level by monitoring temperature(see paragraph 0149, sentence 111). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the inventions of Leddige, Volk, and Fung to create a computer system with memory module monitoring means depending on temperature. The motivation to do so would be to establish an ability to conserve power when there is an unstable temperature issue within a particular memory module.

In reference to claims 62, 88, and 114....

Fung teaches the system, computer system, and method wherein the temperature sensor is operably coupled with at least one memory device to measure a memory device operating temperature(see paragraph 0149, sentence 111).

In reference to claims 63, 89, and 115....

Fung teaches the system, computer system, and method wherein the temperature sensor is operably coupled with each of the memory devices to measure an aggregate memory device temperature(see paragraph 0149, sentence 111).

In reference to claims 64, 90, and 116....

Fung teaches the system, computer system, and method wherein the temperature sensor is operably coupled with the insulative substrate to measure a memory module operating temperature(see paragraph 0149, sentence 111).

In reference to claims 65, 91, and 117....

Fung teaches the system, computer system, and method wherein the temperature sensor is operably coupled with the memory hub to measure a memory hub operating temperature(see paragraph 0149, sentence 111).

In reference to claims 66, 92, and 118....

Fung teaches the system, computer system, and method wherein the temperature sensor further comprises an ambient temperature sensor so that a measured temperature of the memory module can be compared to an ambient temperature(see paragraph 0149, sentence 111 and sentence 117).

In reference to claims 67, and 93....

Leddige discloses the system and computer system wherein the plurality of memory devices comprise a plurality of DRAM devices(see column 2, lines 1-4).

In reference to claims 68, 94, and 119....

Fung teaches the system, computer system, and method wherein the reduced power state comprises a reduced refresh state in which memory cells of the DRAM

devices are refreshed less frequently(see paragraph 0149, sentence 111 and sentences 120-123).

In reference to claims 69, 95, and 120....

Fung teaches the system, computer system, and method wherein the reduced refresh state comprises a self-refresh state(see paragraph 0149, sentence 111 and sentences 120-123).

In reference to claims 70, 96, and 121....

Volk teaches the system, computer system, and method wherein the reduced power state is a reduced response mode in which the module power controller limits response of the memory module to memory commands to control power consumption by the memory module(see column 5, lines 7-15).

In reference to claims 71, 97, and 122....

Volk teaches the system, computer system, and method wherein the module power controller limits the response of the memory module to memory commands by mandating idle intervals between responses to memory commands by the memory module(see column 5, lines 7-15).

In reference to claims 72, 98, and 123....

Volk teaches the system, computer system, and method wherein the output of the activity sensing device communicates that the memory devices of the memory module currently store no programming instructions and data, and the power management controller causes a plurality of devices of the memory module to be powered off(see column 5, lines 7-15).

In reference to claims 73, 99, and 124....

Volk teaches the system, computer system, and method wherein the output of the activity sensing device communicates that the memory devices of the memory module currently store programming information that has not been accessed by the system for an extended period, and the power management controller causes the contents of the memory devices to be saved to a storage device and a plurality of devices of the memory module to be powered off(see column 5, lines 7-15).

In reference to claim 105....

Volk teaches the method wherein the outside control device resides in a memory controller(see column 4, lines 52-55).

In reference to claim 106....

Volk teaches the method wherein the outside control device resides in a system controller(see column 4, lines 52-55).

In reference to claim 107....

Volk teaches the method wherein the outside control device resides in a master memory module(see column 4, lines 52-55).

In reference to claim 108....

Volk teaches the method wherein the outside control device for other memory modules resides within the memory module(see column 4, lines 52-55).

Response to Arguments

5. Applicant's arguments, see Amendments/Remarks, filed 7/30/2007, with respect to the rejection(s) of claim(s) 1-124 under 35 U.S.C. 103(a) as being unpatentable over Leddige et al.(US Patent 6,477,614) in view of Wurzburg et al.(US Patent 5,546,591) further in view of Fung(US PGPub 2005/0177755) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of claims 48-124 under 35 U.S.C. 103(a) as being unpatentable over Leddige et al.(US Patent 6,477,614) in view of Volk(US Patent 5,388,265) further in view of Fung(US PGPub 2005/0177755).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael J. Brown whose telephone number is (571)272-5932. The examiner can normally be reached Monday-Thursday from 7:00am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on (571)272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Michael J. Brown
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SUPERVISORY PATENT EXAMINER
8/16/07